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ASSET commits to developing open embedded instrument tools for the Internal JTAG (IJTAG) standard

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Two experts join ASSET to put development effort on a fast track

Richardson, TX (April 29, 2008) – ASSET® InterTech Inc. (www.asset-intertech.com) is developing and will bring to

market open embedded instrumentation tools based on the preliminary IEEE standard, P1687 Internal JTAG (IJTAG). According to Glenn Woppman, president and CEO of ASSET, the standard is close enough to ratification to begin developing tools.

“Electronics manufacturers are realizing that the external design validation, test and debug technologies which they have now are simply running out of gas,” said Woppman. “As a result, chip vendors as well as the system manufacturers themselves are embedding instruments into silicon. Now, both the chip vendors and system suppliers need open tools to work with these embedded instruments. For the sake of efficiency and agility, these tools must be able to manage embedded instruments from any chip vendor. This is where the IJTAG standard comes in.”

“It is fairly common to develop silicon or tools conforming to a preliminary standard so that manufacturers can become acquainted with the standard before its final ratification. We went through this same process with the original boundary-scan standard (IEEE 1149.1 JTAG) when, as part of Texas Instruments at the time, we committed to developing tools before the standard was actually ratified and, in the long run, we believe we accelerated the adoption rate of boundary scan. As a tools supplier, we think it is critical at this time to send a message to the industry that we will support IJTAG.”

Two Embedded Instrumentation Experts Join ASSET

To put ASSET’s efforts on a fast-track, two well known experts recently joined the company to lead its development of IJTAG tools. Al Crouch, formerly chief scientist and director of DFX research and development at Inovys Corp. of Pleasanton, Calif., and Verigy Ltd. of Cupertino, Calif., has joined ASSET as Chief Technologist, Core Instrumentation. Mr. Crouch has served for the last three years as vice chairman of the P1687 IJTAG working group that is developing the IJTAG standard and has contributed significantly to the hardware architecture definition. Over the last 20 years, he has accumulated vast experience in chip design-for-test at both Freescale Semiconductor (formerly Motorola) and Texas Instruments. Mr. Crouch has filed for more than 30 patents and been granted 15.

In addition to Mr. Crouch, John Potter, formerly the principal automation architect at Inovys Corp. and an engineering supervisor at Motorola Corporation has joined ASSET’s IJTAG tools development effort as Senior Principal Technologist, Core Instrumentation. Mr. Potter is also a more recent member of the

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P1687 IJTAG working group focusing on the language portion. Over the last 18 years in the electronics industry, he has filed for four patents and been granted two.

“A great deal of validation and test instrumentation technology is being embedded into silicon these days,” said Mr. Crouch. “What’s needed now is an open environment that can access all of this volume of embedded instrumentation technology to organize it, schedule its execution, access data collected by the instruments, analyze this data, display results and exert overall control over these embedded technologies. The IJTAG standard, once it is ratified, will provide the foundation for doing this and ASSET is well on its way to providing the open tools that are needed.”

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