



A Whitepaper:
Fault Coverage Reporting

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Table of Contents

Executive Summary	Page 2
Overview	Page 3
Interconnect Test Coverage Report	Page 3
Non-Boundary-Scan Devices	Page 4
ScanWorks Net Classification	Page 5
Net Shorts Fault Coverage Summary	Page 6
Class 1 – Fully Covered	Page 6
Class 2 – Partially Covered	Page 7
Class 3 - Shorts Covered	Page 8
Class 4 - Some Opens Covered	Page 9
Class 5 - Not Covered	Page 10
Class 6 - Covered by Scan Path Verify Actions	Page 11
Interconnect Fault Coverage Report	Page 11
Memory Access Verification Test Coverage	Page 13
Flash Programming Test Coverage	Page 14
Scan Path Verify Test Coverage	Page 16
Combined Fault Coverage Report	Page 16

Executive Summary

One of the challenges of test engineering is knowing when the test is “good enough”. Engineers can spend untold hours and weeks trying to squeeze out one more percentage point of test coverage, but there are always more circuit boards waiting for test generation. There has to be a point where the test is declared “good enough” and the test engineer move on to developing test strategies for the next project. But how does the engineer know to say a certain test or test suite is good enough? The answer, of course, is a fault coverage report which details exactly what problems the tests will detect. This whitepaper describes the fault coverage reporting capabilities of ASSET InterTech’s ScanWorks boundary scan test and programming environment.

Overview

To avoid confusion, this whitepaper begins by defining certain terms. Specifically, we define defects, faults and coverage.

A defect is a mistake in the manufacturing process. For our purposes we are going to limit the discussion to defects that prevent the proper electrical connections between points on a board that should be connected.

During testing, a defect shows up as a fault. A fault is an indication that the results of a test are not the expected results. For example, if a device pin is not properly soldered to the board and electrical contact is not established, a test will find an electrical open, indicated by a stuck-at-1 or stuck-at-0 fault. By diagnosing the fault, the actual defect (improperly soldered pin) can usually be found and fixed. Another example is an unintended electrical connection between two or more pins or nets on a board. The test will find an electrical short, indicated by an unexpected pattern of ones and zeros, while diagnosis will isolate the defect and enable repair. Through testing, we find faults, which, when they are fixed, will eliminate defects. Coverage is a measurement of how many faults your test can find out of the total possible number of postulated faults.

Fault coverage reports give a grade on how well a test detects those faults that it is capable of detecting. The report could describe how well a test covers the entire universe of potential faults, but that is useful only if the test suite is capable of detecting all potential faults. If the test is a boundary-scan scan test, a much more useful report for optimizing this test's coverage is one that concerns itself with only those faults that are detectable by boundary scan. This type of report could provide input to a comprehensive report that includes reports from the other test methods that verify a board was assembled correctly.

Fault coverage reports are also very helpful at determining whether a board has enough testability features designed into it. A certain test may detect 100 percent of all of the defects that it is capable of detecting, but the test method or test technology may only be capable of detecting 10 percent of all of the potential defects on the board. The report can help you by pointing out that you need to design-in additional coverage to take better advantage of the test method.

Faults can be detected directly by boundary scan tests generated specifically to detect faults, or they can be detected by boundary-scan scan operations intended for other purposes. Interconnect tests and Memory Access Verification tests are intended to verify interconnects between devices, while flash programming is intended to read and write data from flash memory. The process of reading and writing data to flash memory results in a test of the interconnects between a boundary scan device and the non-boundary-scan flash memory.

Interconnect Test Coverage Report

Boundary-scan tests can detect shorts and opens on board nets and device pins. The coverage available can be reported as full, partial, or no coverage. The available coverage report can be organized in many ways. For the report to be as useful as possible, you should understand how it was compiled.

ScanWorks interconnect tests are a primary method for verifying that a board is assembled correctly and the electrical connections between devices and the board are working properly. Boundary-scan tests use the test feature built into boundary-scan compliant devices to apply test patterns to the board and verify that the results of the application match the expected results. The test patterns are optimized to provide a thorough level of coverage in the fewest number of patterns. The patterns used to detect two-net shorts are also capable of detecting all “stuck-at” faults. The most commonly used algorithm is known as Wagner patterns or modified Wagner patterns. Extensive discussion of these algorithms is available on the ASSET web site as part of a Boundary Scan Tutorial. (Go to http://www.asset-intertech.com/pdfs/boundariescan_tutorial.pdf to access this tutorial.) Additional types of test patterns such as “Walking Ones and Zeros” can make it easier to diagnose faults, but this topic is beyond the scope of this whitepaper. This paper is focused on detecting faults.

The ScanWorks interconnect fault coverage report documents the coverage obtained with the current input parameters to the Test Pattern Generation (TPG) tools. Test coverage is improved by giving TPG more information to work with through additional models for non-boundary-scan devices or by defining constraints that enable additional testing. In general, to ensure that a net can be tested safely, TPG will not attempt to test a net for which it does not have enough information. Safe testing is defined as having a single driver, boundary-scan or non-boundary scan, active at any time.

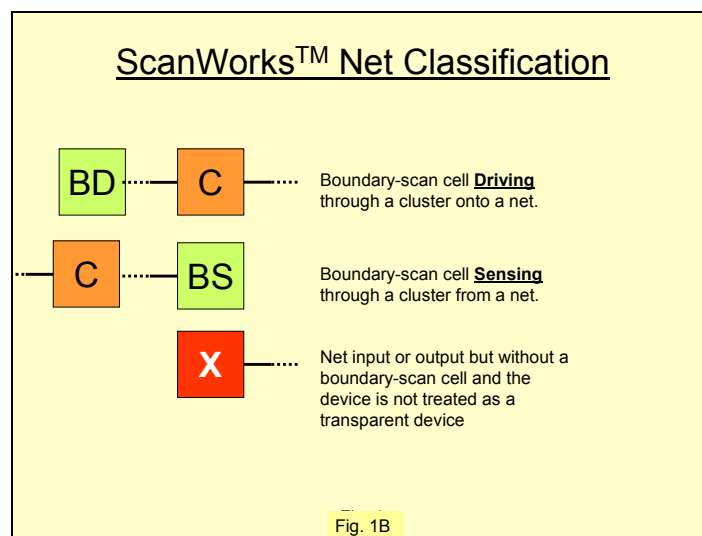
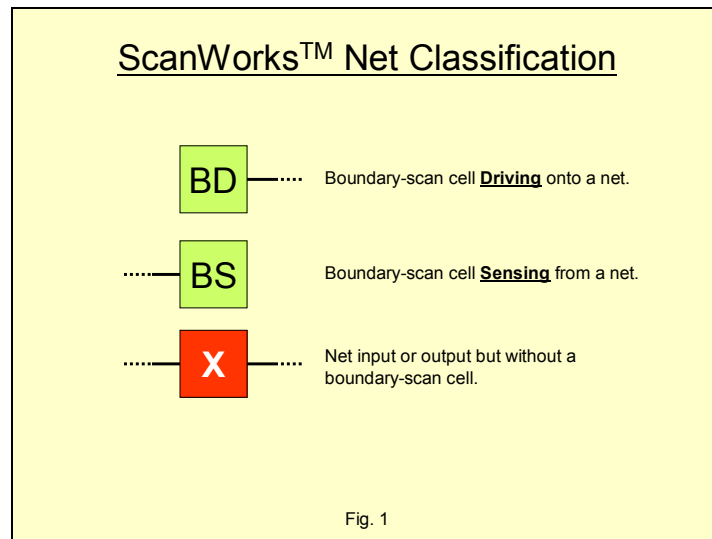
Non-boundary-scan devices

Non-boundary scan (NBS) devices have a tremendous influence on the maximum test coverage achievable via boundary-scan test methods on a typical board. The TPG tools must know if it is safe to test nets with connections to non-boundary scan pins. It is advantageous if the TPG knows that tests can be applied through a NBS device to a boundary-scan device on the other side. The IO characteristics of the NBS device and the “transparency” of the NBS device can be provided manually for each pin, or this can be provided to the TPG in the form of a “cluster” model. A cluster model defines the IO characteristics of each pin on the NBS device and can also describe the input-pin-to-output-pin logic for simple devices. For example, for a ‘245 bi-directional buffer device each IO pin is described as a bidirectional pin with the input-to-output relationship described. The pins that enable the direction and tri-state condition are also defined, enabling the TPG tool to automatically set the control pins to pass boundary scan test patterns through in either direction, assuming the presence of boundary-scan pins on both sides of the ‘245. This can change the available coverage from partial to full coverage on boundary-scan pins and provide coverage of the NBS device’s pins.

The ASSET interconnect TPG creates a fault coverage report based on the information provided by the board netlist, BSDL file information, cluster model data, constraints assigned by the user and user options that select the type of test patterns to use.

ScanWorks Net Classification

The fault information section includes a net shorts fault coverage summary, faults detected by test patterns, test pattern information and calculated faults. We'll use some graphical representations to understand the different conditions possible during boundary-scan testing.



Net Shorts Fault Coverage Summary

The net shorts fault coverage summary provides information on the count and percent of nets within six different classes. The net classification for shorts section of the report provides information about which nets fall within each classification. The net shorts fault coverage summary is based solely on the testing done during the last boundary-scan configuration and only present if Wagner patterns are chosen for that configuration.

Class 1 - Fully Covered

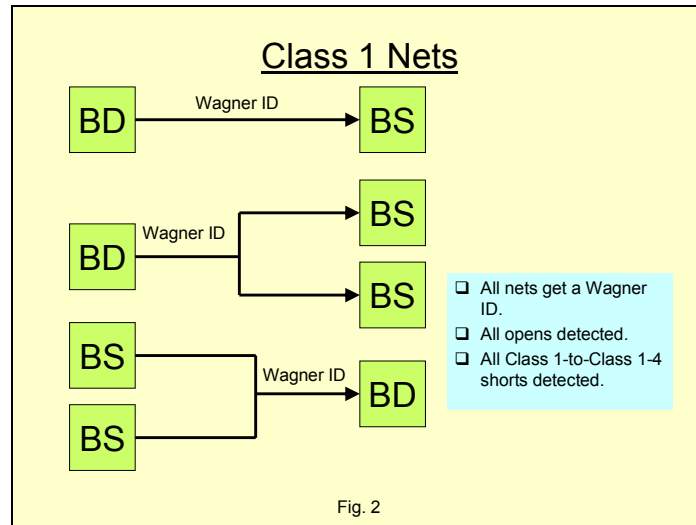
This class includes nets that have full opens coverage for all pins on the net and full shorts coverage to all other nets that have shorts coverage (Classes 1-4). Class 1 nets can also include those that are joined, equal or inverted to a class 1 net.

A net has class 1 shorts coverage if:

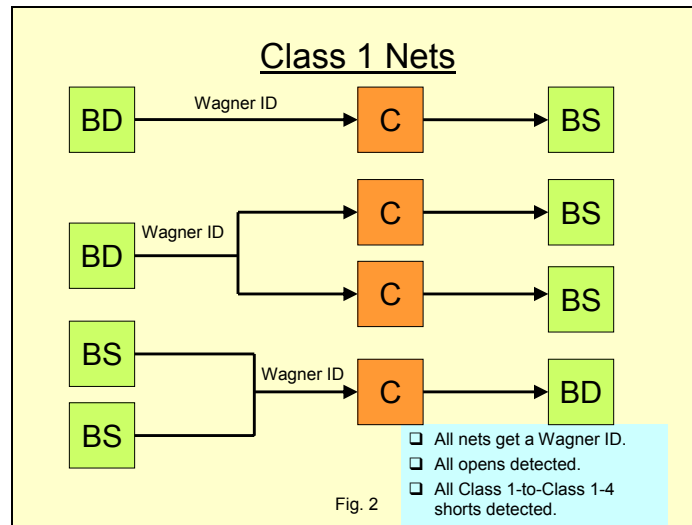
- The net gets a complete Wagner pattern set
- The net is observed during all steps of the Wagner patterns (either directly or because it has the input of a transparent device)
- The net is driven by a boundary-scan output or a cluster output
- The net has no extraneous pins (that is, pins not related to write cell to read cell relationship). Test points (single-pin devices) are allowed, but connectors are not.

Possible configurations of class 1 nets are:

With no cluster device connection:



With cluster device connections:



Notes: Class 1 nets can be single-drive single-sense, or single-drive multiple-sense, or multiple-drive (i.e. onto a bus) single-sense, but in all cases each drive point and sense point must contain a boundary-scan cell. “Getting a Wagner ID” means that the nets go into the pool of nets to be assigned a Wagner code for interconnect test.

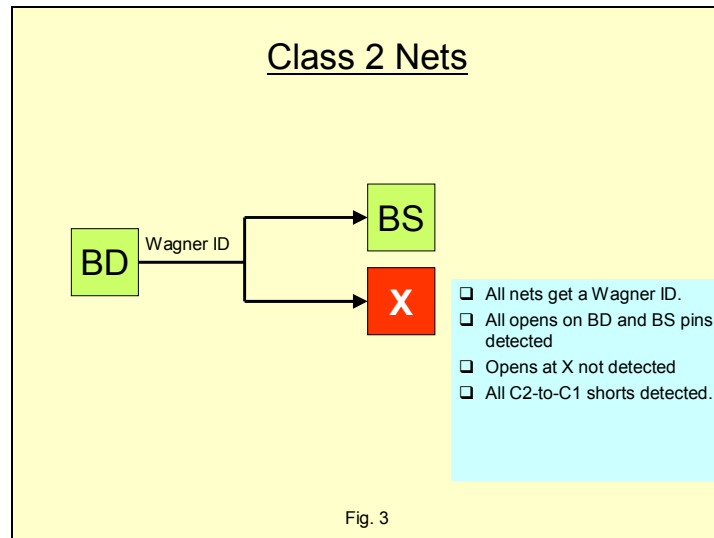
Class 2 - Partially Covered

This class includes nets that have full shorts coverage, but opens coverage is not present for all pins. Class 2 nets can also include those that are joined, equal, or inverted to a class 2 net. A net has class 2 shorts coverage if:

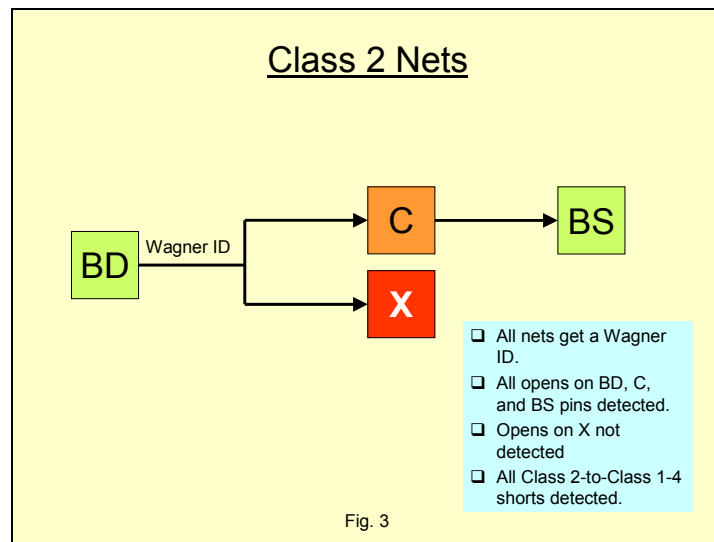
- The net fails to meet the requirements for class 1
- The net gets a complete Wagner pattern set
- The net is observed during all steps of the Wagner patterns (either directly or because it has the input of a transparent device)
- The net is driven by a boundary-scan output or a cluster output.

Possible Class 2 net configurations:

With no cluster device connections:



With cluster device connections:



Notes: Full shorts coverage to all class 1-4 nets. Opens coverage on BD, C, and BS pins, as shown in the diagram. No opens coverage on X.

Class 3 - Shorts Covered

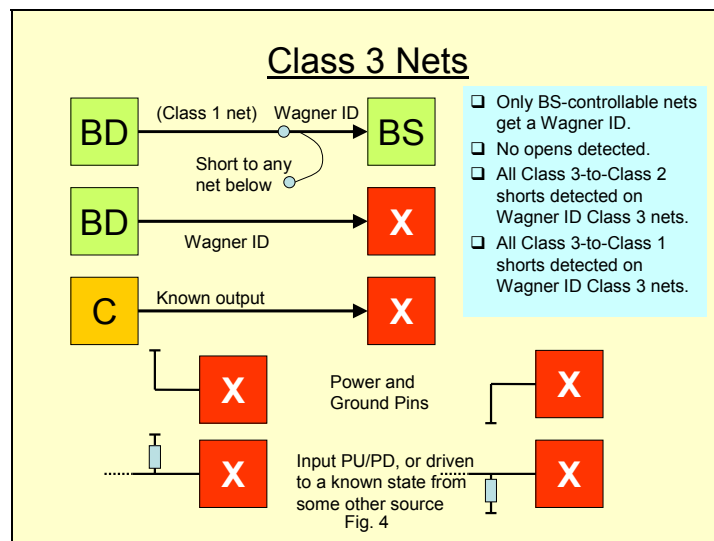
This class includes nets where the shorts coverage is indirect (that is, faults must be detected at the other net to which it is faulted, which requires the other net must have a BS pin.), and is only determined versus nets that fall into class 1 or class 2. Class 3 nets can include:

- Nets that actively participate in shorts testing (in which case shorts to class 4 nets are covered)
- Power/ground nets
- Nets driven to a constant value
- Nets that are constantly pulled up or pulled down
- Nets that are driven to a known state by a cluster output

A net has class 3 coverage if:

- The net fails to meet requirements for classes 1, 2 and 4
- The net has a known state at all test steps (held to a static value or driven by cluster output, or pulled up/pulled down)
- The net's value is not observable at all test steps

Possible Class 3 nets:



Class 4 - Some Opens Covered

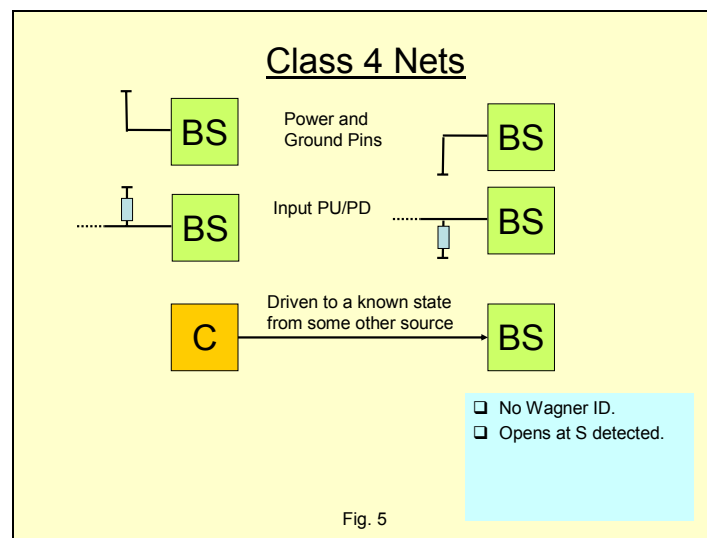
This class includes nets whose coverage for opens is direct (has a boundary-scan receiver), but is only determined versus nets that are driven to a constant value, and nets that are constantly pulled down or driven to a fixed/ known state. Class 4 nets can include:

- Power/ground nets
- Nets driven to a constant value
- Nets that are constantly pulled up or pulled down
- Nets that are driven to a known state by a cluster output

The values on class 4 nets must be observable at every test step by a boundary-scan receiver that is directly connected, or is connected through one or more transparent devices. A net has class 4 coverage if:

- The net fails to meet requirements for classes 1 and 2
- The net has a known state at all test steps (held to a static value or driven by cluster output, or pulled up/pulled down)
- The net does not get a complete Wagner pattern set
- The net's value is observable at all test steps (has boundary-scan receiver or is sensed through pull device (power/ground nets only) or drives a cluster input/clock whose output is sensed)

Possible Class 4 nets:

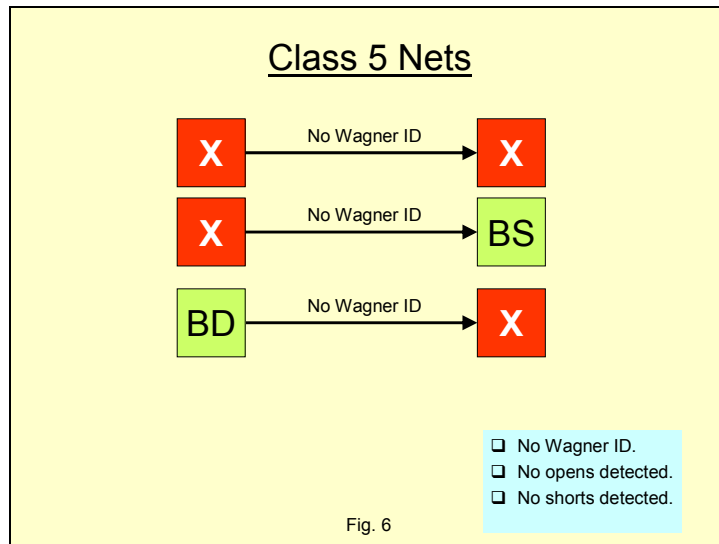


Notes: Shorts are not covered because of the lack of Wagner patterns

Class 5 - Not Covered

This class includes nets where coverage cannot be guaranteed due to not meeting any of the criteria specified by the other classes.

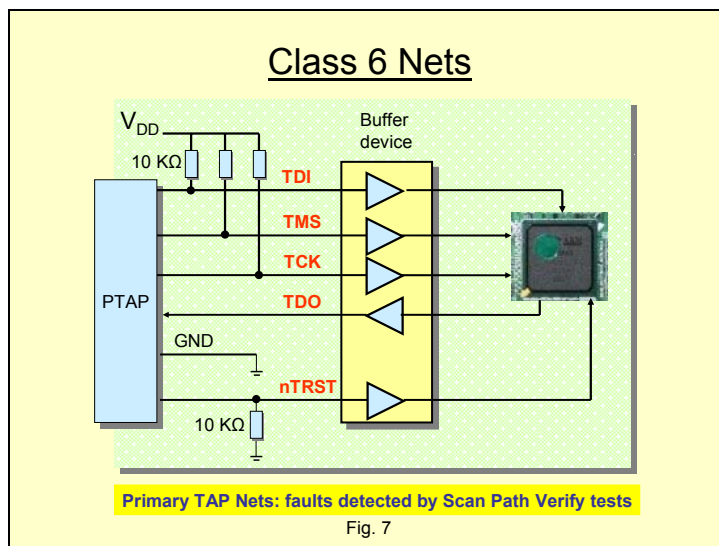
Possible Class 5 nets:



Class 6 - Covered by Scan Path Verify actions

A net has class 6 coverage if the net is associated with TAP pins on boundary-scan devices in the active chain(s).

Possible Class 6 nets:



Interconnect Fault Coverage Report

Example Report:

Interconnect Fault Coverage		
Boundary Scan Pin Fault Coverage		
BScan Pin Fault	69.62%	
Net Short Fault Coverage Summary		
	Nets	
Class	Count	Percent
1 (Fully covered opens and shorts by Wagner patterns)	12	1.4
2 (Partially covered: full shorts but not full opens)	251	28.7
3 (Shorts covered but no opens covered)	229	26.2
4 (Some shorts covered)	36	4.1
5 (No shorts or opens covered)	342	39.1
6 (TAP nets: covered by Scan Path Verify)	5	.6
Total	875	100.0

Fig. 8 Overall net coverage is 36.8%

Overall Net Coverage is the percent of all nets on the board that have been identified to have at least one boundary-scan read cell or write cell on the net. Based on the net Class definitions, this includes all Class 1, all Class 2, some Class 3 and some Class 4. In the example above, all Class 1 + all Class 2 = 30.1%. Adding in the Class 3s and 4s takes the total to 60.4%. The actual figure is 36.8% which is > 30.1% (as it should be) but < 60.4% (again, as it should be). In the example, there are many Class 3 and 4 nets that do not have boundary-scan cells on them.

Boundary Scan (BScan) Pin Fault Coverage indicates the percentage of all possible boundary-scan faults that would be detected by the interconnect test. All possible boundary-scan faults includes the following where “Read” is the equivalent of “Sense” and “Write” is the equivalent of “Drive”:

- Each pin with a BSCAN Read cell has two BSCAN Read (Sense) Faults (BRF)
 - BRF-Stuck-At-0 (BRF-SA0)
 - BRF-Stuck-At-1 (BRF-SA1)
- Each pin with a BSCAN Write (Drive) cell has two BSCAN Write Faults (BWF)
 - BWFStuck-At-0 (BWF-SA0) and
 - BWF-Stuck-At-1 (BWF-SA1) (of course,
- If a pin has both Read and Write cells, all four faults are enumerated

Detected faults include stuck-at-1 and stuck-at-0 opens plus all 2-net shorts between all nets that have received a Wagner ID i.e. come within the range of the Wagner patterns. Some opens and shorts will not be detected i.e. some opens on Class 2 nets and all opens on Class 3 nets. Therefore, the percentage will always be less than 100% if Class 2 and Class 3 nets are identified.

Concerning coverage, if any patterns are generated for which a Read (Sense) cell is expected to be 0, then the BRF-SA1 for that pin is considered to be covered. Similarly, if

any patterns are generated for which a Read (Sense) cell is expected to be 1, then the BRF-SA0 for that pin is considered to be covered.

With respect to pins with Write (Drive) cells:

- IF any patterns are generated for which a Write (Drive) cell asserts a logic 0 at its connected net
- AND at least one pin with a Read (Sense) cell is connected to the same net
- AND at least one of those Read (Sense) cells is expected to be 0,
- THEN the BWF-SA1 for that pin is considered to be covered.

Similarly,

- IF any patterns are generated for which a Write cell asserts a logic 1 at its connected net
- AND at least one pin with a Read cell is connected to the same net
- AND at least one of those Read cells is expected to be 1,
- THEN the BWF-SA0 for that pin is considered to be covered.

Relating this to classes 1-4 –

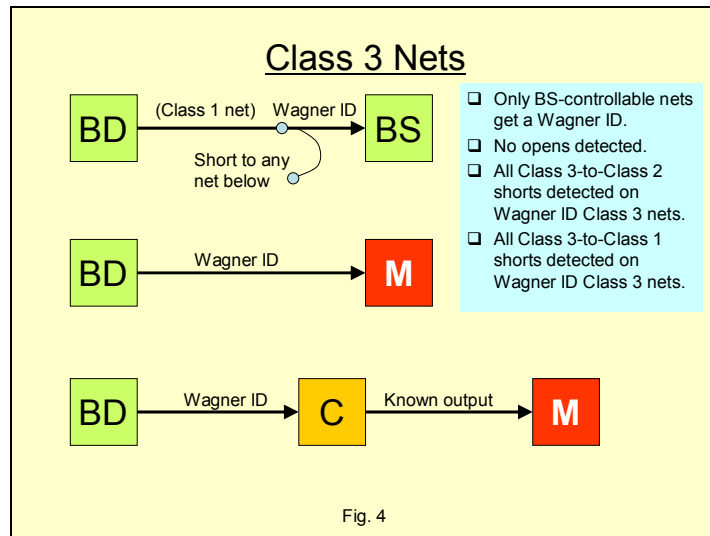
- A pin with a BSCAN Read (Sense) cell on a Class 1 or Class 2 net will have coverage for both BRF-SA0 and BRF-SA1 faults;
- A pin with a BSCAN Write (Drive) cell on a Class 1 or Class 2 net will have coverage for both BWF-SA0 and BWF-SA1 faults;
- A pin with a BSCAN Read (Sense) cell on a Class 4 net will have coverage for only one of BRF-SA0 or BRF-SA1 (depending on whether the pin is fixed high or low, respectively);
- A pin with BSCAN Write (Drive) cell on a Class 4 net will have coverage for only one of BWF-SA0 or BWF-SA1 (depending on whether the pin is fixed high or low, respectively);
- Faults at BSCAN pins connected to nets in Class 3 or Class 5 or Class 6 are not covered.

The Interconnect Report has much more information in it, describing coverage at the net and pin level, the types of faults detected and much more. A detailed description will be provided in another white paper.

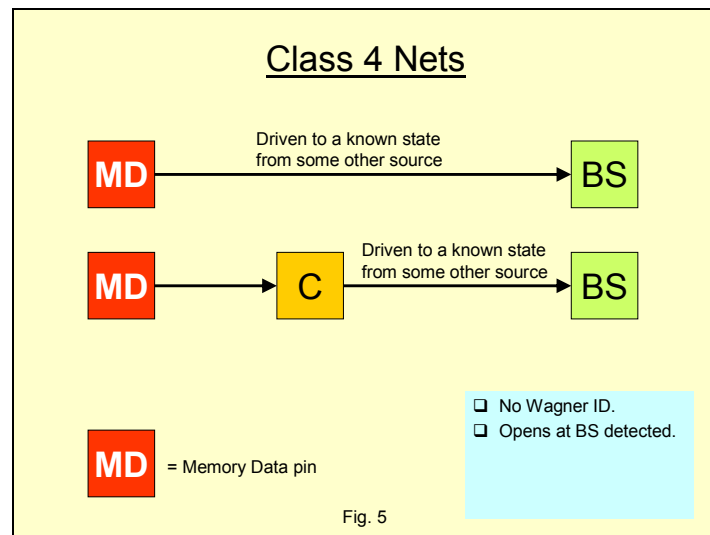
Memory Access Verification Test Coverage

Memory Access Verification verifies that the connections between a boundary-scan device and memory devices are not defective. Test data is written to the memories and then read back by controlling the data, address and control signals via boundary-scan cells in adjacent boundary-scan devices. Patterns of data are written to enough addresses to ensure that any shorts or opens are detected.

Because the data, address and control signals are driven by boundary-scan cells, these signals are covered for shorts by interconnect tests as class 3 nets. The nets may be connected directly to the memory device or through a cluster device.



The data signals are covered for opens as class 4 nets by the memory access verification tests.

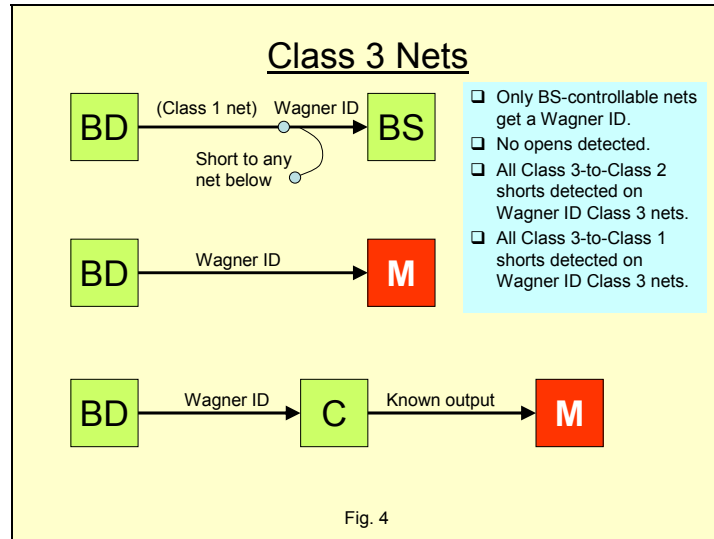


The address and control signals are covered for opens by the Memory Access Verification test as a result of verifying correct operation. If any pin was open, the expected data would not be read from the memory. These pins can be classified as class 4 pins.

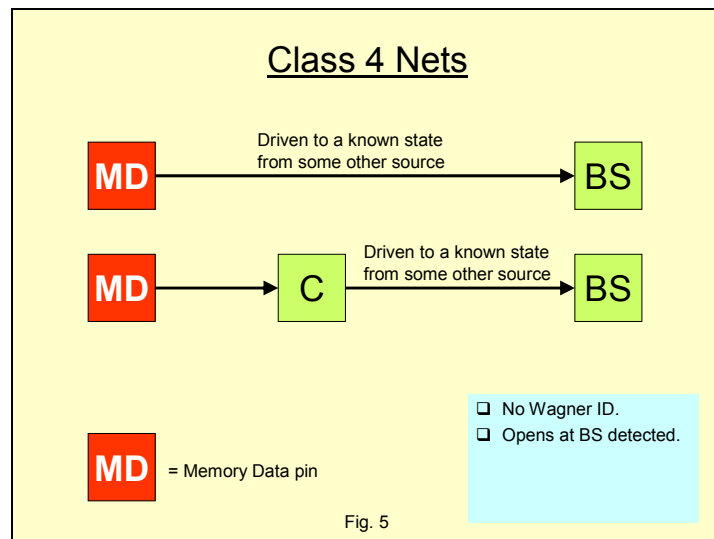
Flash Programming Test Coverage

Flash programming verifies that the connections between a boundary-scan device and flash memory devices are not defective. Before programming operations start, test data is written to the memories and then read back by controlling the data, address and control signals via boundary-scan cells in adjacent boundary-scan devices. Patterns of data are written to enough addresses to ensure that any shorts or opens are detected.

Because the data, address and control signals are driven by boundary-scan cells, these signals are covered for shorts by interconnect tests as class 3 nets. The nets may be connected directly to the memory device or through a cluster device.



The data signals are covered for opens as class 4 nets by the flash programming tests.



The address and control signals are covered for opens by the flash programming test as a result of verifying correct operation. If any pin was open, the expected data would not be read from the flash memory. These pins can be classified as class 4 pins.

Scan Path Verify Test Coverage

Verifying the scan path is an operation that essentially “tests the tester.” If the scan path is not working, the interconnect test cannot be expected to provide any coverage of the TAP signals.

The ScanWorks Scan Path Verification action can optionally include seven separate tests. However, the first one is usually sufficient to verify the scan path infrastructure. It starts with a Test Logic Reset operation to put all boundary-scan devices in a known state, with either the BYPASS or IDCODE register in the scan path. A Data Register scan is executed and the results are compared with the expected data for the expected scan path configuration based on the current design description. If this fails, there could be several problems, including an incorrect design description, an incorrect BSDL file for a device, a second source device with a different IDCODE than expected or an actual defect in the TAP signals.

Any open or short on any TAP signal will be detected by the scan path verification test, providing class 1 coverage on each signal. These signals include all the TDO-to-TDI connections between the primary IO and between each device as well as the TMS and clock signals. A TRST test available in the Scan Path Verification action provides class 1 coverage for the TRST TAP signal by running a functional test on the reset process.

Combined Fault Coverage Report

The combined fault coverage report can create one report that includes the coverage from Scan Path Verify, Interconnect Test, Memory Access Verification and Flash programming actions. The user selects the actions to be included in a report which enables them to create a report for the coverage available with a specific set of actions.

The format and contents of the Combined Fault Coverage report will be described in another white paper.