Test Tips

A continuing series of tips to enable users of ASSET InterTech's ScanWorks boundary-scan test and programming environment to get the most from their investment.

Automation in ScanWorks 3.3 increases user productivity

No: 301
Date: April 2003
© ASSET InterTech, Inc.

Introduction

Significant productivity improvements like more effective netlist merging, and improved automatic interconnect and memory test generation have been incorporated into ScanWorks 3.3 to streamline the test development and application process. Other enhancements include the ability to simultaneously generate multiple memory interconnect tests and automatically create a sequence of tests for production, support for testing multiple units at once, and the addition of a Process Automation Scripting API and a web-based model library. This Test Tip focuses on the improvements in productivity that users of ScanWorks will see from enhancements to netlist merging, and automatic interconnect and memory test generation.

Tests on a customer's motherboard/daughtercard assembly using ScanWorks 3.3 third-generation technology demonstrated a dramatic improvement in test generation and test build times over ScanWorks' second generation technology, reflecting an increase in user productivity anywhere from 1.5x to 9.3x. In addition, the ability of ScanWorks 3.3 to automatically detect unsafe conditions and generate test constraints affected productivity by decreasing safe test generation time and by reducing the likelihood of damaging a printed circuit board.

Customer Board Description

The customer's board consisted of a motherboard and 35 daughtercards of two different types. Both types of daughtercards consisted mainly of memory devices with boundary-scan buffers. Following an automated netlist merge by ScanWorks 3.3, the total number of nets for the entire motherboard/daughtercard assembly was 14,068. The following table shows the basic characteristics of the assembly:

	Nets	Devices	Scannable Devices	Memory Devices	Types of Memory
Motherboard	9,172	1,050	2	0	0
Daughtercard 1 (32 cards)	18,976	4,800	32	32	1
Daughtercard 2 (3 cards)	1,833	477	3	6	1
Totals	29,981	6,327	37	38	2
Total after merge	14,068				

Test Generation

Several different types of actions were generated and executed on this assembly. These included:

- Merging the netlists of the motherboard and daughtercards.
- Generating and building interconnect tests for all of the boundary-scan devices in the assembly.
- Generating and building interconnect tests for the non-boundary-scan memory devices in the assembly.

The tests were run in two different boundary-scan environments. First, the automatic test program generation (ATPG) capabilities of ScanWorks' second-generation's boundary-scan engine were used as a benchmark. Second, the same tests were generated and executed in the ScanWorks 3.3 third-generation environment to determine the effects that ScanWorks 3.3 would have on user productivity. The results were as follows:

Type of Action	Benchmark Generate and Build Times	ScanWorks 3.3 Generate and Build Times	Increase in Productivity	Time saved
Merge Net Lists	56 hours	6 hours	9.3x	50 hours
Boundary Scan Interconnects	12 hours, 26 minutes	8 hours, 4.5 minutes	1.5x	4 hours, 21.5 minutes
Memory Interconnects	1 hour, 2.5 minutes	8 minutes	7.8x	54 minutes

Net List Merging

A new netlist merging tool in ScanWorks 3.3 simplifies the testing of motherboard/daughterboard assemblies by making it easier to specify the nets to be merged and by improving the efficiency of the merge algorithm. Merging is now accomplished within the standard ScanWorks netlist import dialog and it is driven by a simple command file.

Boundary-Scan Interconnect

The interconnect test ATPG tool in previous generations of ScanWorks has been replaced in ScanWorks 3.3 by a new interconnect ATPG tool that was developed and is supported by ASSET. Because the company has developed this tool, ASSET can make improvements quickly, increasing user productivity accordingly. In ScanWorks 3.3, better use of non-boundary-scan models for automatic constraint generation and a more

efficient test generation process has reduced interconnect test generation time significantly.

Safety Issues

Boundary-scan tests that are automatically generated by a boundary-scan test system sometimes can damage the board-under-test unless certain conditions, such as bus conflicts, are avoided. Besides testing the effects that the third-generation ScanWorks has on the productivity of test engineers and technicians, additional conclusions were drawn regarding the safety of tests generated in the ScanWorks 3.3 environment when compared to the benchmark second-generation ScanWorks environment.[1] These conclusions are based on the following facts:

- The handling of cluster models of non-boundary scan devices is much more sophisticated in ScanWorks 3.3. For example, ScanWorks' ability to drive through complex non-boundary scan devices like memories yields better fault coverage and eliminates the need to manually generate some cluster tests.
- ScanWorks 3.3 automatically avoids bus conflicts by inserting constraints to disable non-bounary-scan device outputs. Some boundary-scan environments require manual intervention for the insertion of these constraints, increasing the chance of human error and unsafe tests.
- ScanWorks 3.3 automatically detects unsafe conditions and warns the user before an action is taken. Some boundary-scan test systems do not inform the user of unsafe conditions until a fault coverage report is built.
- In ScanWorks 3.3, constraints built into a device-level cluster model will automatically be reflected at the board level, avoiding the chance of human error or neglect.

Test Coverage

Because of the design-for-test practices followed by the customer in this case, the boundary-scan test coverage was very high for this motherboard/daughtercard assembly. In fact, all of the devices on the two daughtercards were boundary scan compliant. This yielded a boundary-scan test coverage in the range of 95 to 99 percent. The test coverage was equivalent with both tools.

Memory Device Models

Each of the two types of daughtercards were populated with one type of memory device. One daughtercard consisted of static random access memory (SRAM) while the other featured synchronous dynamic random access memory (SDRAM). To test the interconnection of these memory devices, the customer was able to download the device models from ASSET's web library, eliminating the need to manually characterize the devices or to manually generate macros that would initialize, write and read to these devices. The device models from ASSET's web library streamlined this process to the

point where the benchmark memory interconnect testing was reduced from one hour, 2.5 minutes to just eight minutes with ScanWorks 3.3.

Since these benchmarks were run, an additional feature has been implemented to enable the generation of multiple memory interconnect actions at once, avoiding the need to manually create 35 individual memory interconnect actions. The eight minute test generation time can potentially be reduced to a few seconds.

Summary

ASSET is constantly working to make users more productive. The goal is to enable an experienced ScanWorks user to create and debug a full set of boundary-scan tests in one day or less. It is clear that significant productivity gains are possible with the latest release of ScanWorks. In addition, ScanWorks' return on investment is outstanding because updates and enhancements are available at no cost to customers who have a maintenance contract.

1. *"Why the ScanWorks Release 3.2 Interconnect ATPG has the Capability to Produce Safer Interconnect Vectors than the VICTORY-Based APTG in Release 3.1.1"* By Self-Test Services, 10/18/02.